Model 560-5208
E1/T1 Reference Interface

SECTION ONE

1. FUNCTIONAL DESCRIPTION

1.1. PURPOSE OF EQUIPMENT

The TrueTime 560-5208 E1/T1 Reference Interface is a plug-in option card for the Model 56000 DRC. This option card offers the user one reference output phase-locked to one of two T1 or E1 AMI signals.

The input signals from the backplane buss-isolated passive inputs A and B (1.544 MHz T1 or 2.048 MHz E1) are selectable by on-card DIP switch SW1 position 4. The clocks are extracted from the two raw AMI input signals and converted into a TTL clock via two DALLAS DS2187 Receive Line Interfaces. (See page 5 of 6 of the schematics). The TTL clock signals are received via the internal multiplexer of U16, which passes primary input A or secondary input B. If the primary signal A is faulty or lost, the multiplexer shifts to signal B and the phase locked loop locks to input B. If the primary signal returns no faults, the input can be set back to primary via CPU commands.

A local 10 MHz signal is phase-locked to the selected input signal and can be inserted on one of five reference bus lines (A, B, C, 7F, or 8F). This 10 MHz signal can be converted to 5 MHz or 1 MHz before being introduced to the reference bus for total flexibility between various 56000 chassis configurations.

1.2. PHYSICAL SPECIFICATIONS

Dimensions:	0.8”w X 3.94”h X 8.66”d (2 cm X 10 cm X cm)
Weight:	Approximately ¼ pound (1/8 kg)

1.3. ENVIRONMENTAL SPECIFICATIONS

Operating Temp:	0° to +50°C
Storage Temp:	-40° to +85°C
Humidity:	95% relative, non-condensing
Cooling Mode:	Convection
Altitude:	10,000 ft. ASL

1.4. POWER REQUIREMENTS

Voltage:	18-72 VDC
Power:	3W

1.5. FUNCTIONAL SPECIFICATIONS

1.5.1. INPUTS A AND B

Signal Type:	AMI E1 or T1
Input Voltage Swing:	-7.0 to 12V
Minimum Sensitivity:	1 Vpk
Frequency:	1.544 MHz or 2.048 MHz (switch-selectable)
Accuracy:	±1 PPM
Input Impedance:	
T1:	100 ohms
E1:	75 ohms or 120 ohms (jumper selectable)
Jitter:	0.05 UI @ 10 Hz

1.5.2. OUTPUT (to Backplane)

Frequencies:	1, 5 or 10 MHz
Frequency Accuracy:	Equal to Reference on E1 or T1 Input
Frequency Stability:	
Long-Term:	Equal to E1 or T1 Reference on Primary or Secondary.
Short-Term:	$< 1 X10^{-9}$ (1 s avg., ref $1X10^{-10}$)
Signal When Configured For 1 and 5 MHz:	
Type:	Squarewave
Amplitude:	4 Vp-p into 50 ohms.
Signal When Configured For 10 MHz:	
Type:	Sinewave
Amplitude	3 Vp-p into 50 ohms

1.5.3. CARD COMPATIBILITY

Location:	Slots 1-17
Compatibility:	Must have specified input board in corresponding rear slot.

SECTION TWO

2. INSTALLATION AND OPERATION

2.1. HOT SWAPPING

All cards, input cables, and output cables are hot swappable. It is not necessary to remove chassis power during insertion or removal. Hot swapping and reference-source changes are abrupt, the effects difficult to characterize; however, the system is designed to protect against permanent effects and minimize temporary effects of these events. Typically, adjacent-card hot swapping has a negligible effect on the E1/T1 Reference Interface. The effect of redundant power supply switchover is also negligible.

The effect of a reference-source change is less predictable. The reference frequency is delivered via Passive I/O Interface inputs A and B. If the A reference is lost, the Synthesizer locks to the B reference. However, since the E1/T1 input signals are not bussed on the chassis backplane, a failure of the E1/T1 Reference Interface Board would result in a system reference failure. This can be avoided if a second 560-5208 assembly is installed in the same chassis with another E1/T1 reference connected to a second Passive I/O Interface installed in the corresponding rear slot. The reference system would then be considered to be dual redundant**.**

2.2. REMOVAL AND INSTALLATION

CAUTION: Individual components on this card are sensitive to static discharge. Use proper static discharge procedures during removal and installation.

Refer to CARD COMPATIBILITY section prior to installing new card.

To remove card, loosen the captive retaining hardware at the top and bottom of the assembly, then firmly pull on the handle at the bottom of the card. Slide the card free of the frame. Refer to the SETUP section for any required switch settings; or, set them identically to the card being replaced. Reinstall the card in the frame by fitting it into the card guides at the top and bottom of the frame and sliding it in slowly, avoiding contact between bottom side of card and adjacent card front panel, until it mates with the connector. Seat card firmly to avoid contact bounce. Secure the retaining screws at the top and bottom of the card assembly.

2.3. SETUP

The setup of the 560-5208 E1/T1 Reference Interface card involves setting the following jumpers and DIP switches.

2.3.1. JUMPER SETTINGS

The setup of the 560-5208 involves selection of the following jumper positions.

2.3.1.1. INPUT TERMINATION JUMPERS (JP1 - JP12)

All termination jumpers should be set according to the tables below.

JUMPER/ SIGNAL	**JP1**	**JP2**	**JP3**	**JP4**	**JP5**	**JP6**
T1 (100O)	2-3			2-3		
E1 (75O)		2-3			2-3	
E1 (120O)			2-3			2-3

JUMPER/ SIGNAL	**JP7**	**JP8**	**JP 9**	**JP10**	**JP11**	**JP12**
T1 (100O)	2-3			2-3		
E1 (75O)		2-3			2-3	
E1 (120O)			2-3			2-3

2.3.1.2 SINGLE-ENDED (UNBALANCED) INPUT JUMPER (JP14 AND JP15)

Grounding jumpers are provided for single-ended or unbalanced E1/T1 inputs connected to the 560-5208. Refer to the table below for proper configuration of jumpers JP14 and JP15.

JUMPER/ SIGNAL	**JP14**	**JP15**
BALANCED	1-2	1-2
UNBALANCED	2-3	2-3

2.3.2. SWITCH SETTINGS

2.3.2.1. SWITCH (SW1) REFERENCE OUTPUT FREQUENCY SELECT AND RECEIVE CLOCK SELECT

Sections 1, 2, and 3 of this switch provide selection for the output frequency to be inserted on the backplane reference bus. The available frequencies are 1, 5, and 10 MHz. The table below shows the proper switch position for each of the three frequencies.

SWITCH/ FREQUENCY	**SW1-1**	**SW1-2**	**SW1-3**
10 MHz	ON	OFF	OFF
5 MHz	OFF	ON	OFF
1 MHz	OFF	OFF	ON

Section 4 of this switch selects the input as either a T1 or E1 signal. The table below shows the proper switch position for these two choices.

SWITCH/ SIGNAL TYPE	**SW1-4**
E1	ON
T1	OFF

2.3.2.2. SWITCHES (SW2 AND SW4) FOR 10 MHz SINEWAVE REFERENCE BUSS SELECT

To select a 10 MHz sine wave signal to be inserted on the one Reference Buss line, sections 1, 2, and 3 of SW2 should be set OFF; and SW4 should be set to one of five possible settings shown below.

SWITCH/ OUTPUT	**SW4-1**	**SW4-2**	**SW4-3**	**SW4-4**	**SW4-5**	**SW4-6**	**SW4-7**	**SW4-8**
REFA	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
REFB	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF
REFC	OFF	OFF	ON	OFF	OFF	ON	ON	OFF
7F	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
8F	OFF	OFF	OFF	OFF	ON	ON	OFF	ON

2.3.2.3. SWITCHES (SW2 AND SW4) FOR 1 AND 5 MHz REFERENCE BUSS SELECT

To select a 1 or 5 MHz squarewave signal to be inserted on the one Reference Buss line, sections 1, 2, 3, 4, and 5 of SW4 should be set OFF. Sections 1, 2, and 3 of SW2 select the reference bus line that will be driven by the output of the 560-5208. This squarewave signal can drive one and only one of the backplane bus lines REFA, REFB, REFC, 7F, or 8F. The proper switch positions to select each of the five possible settings are shown in the tables below:

SWITCH/ OUTPUT	**SW2-1**	**SW2-2**	**SW2-3**
REFA	ON	OFF	OFF
REFB	OFF	ON	OFF
REFC	ON	ON	OFF
7F	OFF	OFF	ON
8F	ON	OFF	ON

2.3.2.4. OUTPUT DISABLE OPTION SWITCH (SW2-4)

For squarewave output only: When SW2-4 is in the "ON" position the output inhibit option is enabled. With this option selected, the reference output signal (1, 5, or 10 MHz) is shut off when both primary and secondary E1/T1 signals fail.

SWITCH/OUTPUT STATUS IF NO INPUT AVAILABLE	**SW2-4**
FLYWHEEL	OFF
DISABLE	ON

2.3.2.5. ZERO CODE SUPPRESSION AND OPTION SWITCH (SW3-1)

Set SW3-1 to the "OFF" position to enable Zero Code Suppression (ZCS). This will cause B8Z3 coded signals (for T1 applications) or HDB3 coded signals to be replaced with all zeros, therefore disabling detection of bipolar violations.

SWITCH/MODE	**SW3-1**
ZCS ENABLED	OFF
ZCS DISABLED	ON

2.3.2.6. SECONDARY DISABLE SWITCH (SW3-2)

Set SW3-2 to the “ON” position to disable the secondary E1/T1 channel. This will disable fault output reporting and any secondary channel activity.

SWITCH/MODE	SW3-2
SECONDARY ENABLED	OFF
SECONDARY DISABLED	ON

Switches SW3-3, and 4 should all be set to the “OFF” position. Their use is reserved for future enhancements to the cards functionality.

2.4. FAULT INDICATIONS

All indicators activate briefly following hot-insertion or power-up. This normal condition occurs as the card configures itself. The following paragraphs describe operation during post power-up conditions.

2.4.1. POWER SUPPLY / REFERENCE FAULT

A P/S LED continuously flashing at 1 PPS indicates that a fault is present with the Secondary E1/T1 input (I/O line B) as well as the Primary input; or that the local oscillator has drifted such that its voltage control has drifted out of range. Because of the long warm-up period of the local oven oscillator, this LED may begin to blink immediately after power-up. For this reason a primary to secondary fault switch may occur if a valid secondary input is connected to the input interface. If this happens, wait until the LED ceases blinking for a period of at least 30 seconds before invoking the “PRI” command via the CPU. In systems which do not include a secondary input to the 560-5208, the LED may blink for the same reason; however since a switch will not occur, the user should invoke a “CL” command to clear any latched faults 30 seconds after the LED ceases blinking.

A solid LED indicates a local power supply failure. An extinguished power supply LED indicates that the PLL is locked to one of the incoming E1/T1 signals.

2.4.2. INITIALIZATION FAULT

This on-card fault indicator is not externally visible, although it can be seen by installing the card next to an empty slot. It indicates a failure of the card to initialize properly during power-up. Activation of this LED is accompanied by activation of all of the front panel indicators. Occasionally, this fault is caused by a temporary condition related to the cycling of power and can be cleared by a

power or hot swap cycle. If this is unsuccessful, the card is defective.

2.4.3. DETAILED STATUS VIA CPU

The Fault Monitor CPU has access to detailed 560-5208 card status. When the CPU card provides the verbose mode serial report, fault status is available in a 2-byte format, with each binary nibble displayed as a hexadecimal (HEX) character.

The Verbose report displays the Fault status. In this context, a reported fault indicates a problem. The Machine report, when used, reports the current status (settings) of the switches and faults in hexadecimal characters. Together, they pinpoint problems and help the technician view the switch settings on the cards without removing them.

2.4.4 VERBOSE REPORTS

The following is an example of a Fault Monitor CPU report in Verbose mode:

```
TrueTime 56000 Site 01
Automatic Reports Enabled
Periodic Reports Disabled
Primary Inputs Selected REFA No REFB No REFC Off PRI OK SEC OK TER Off

1. Undefined        OK        Undefined      OK
2. Undefined        OK        Undefined      OK
3. 5208 XL2 LOCAL OSC FAULT 0407 Undefined OK
4. Undefined        OK        Undefined      OK
```

The above sample tells you that:
Automatic reports are enabled and Periodic reports are disabled.
Primary inputs REF A and REF B are not bussing the Aux. Ref.
REF C is off. Primary and Secondary inputs OK, Tertiary is OFF.
Numbers 1-4 are slots (not all slots are shown in the example).
Slots 1,2,and 4 are undefined (empty) and functional (OK).
Slot 3 is read as follows:
5208-1 is the abbreviation of the 560-5208-1 card. The fault reading is 0407.

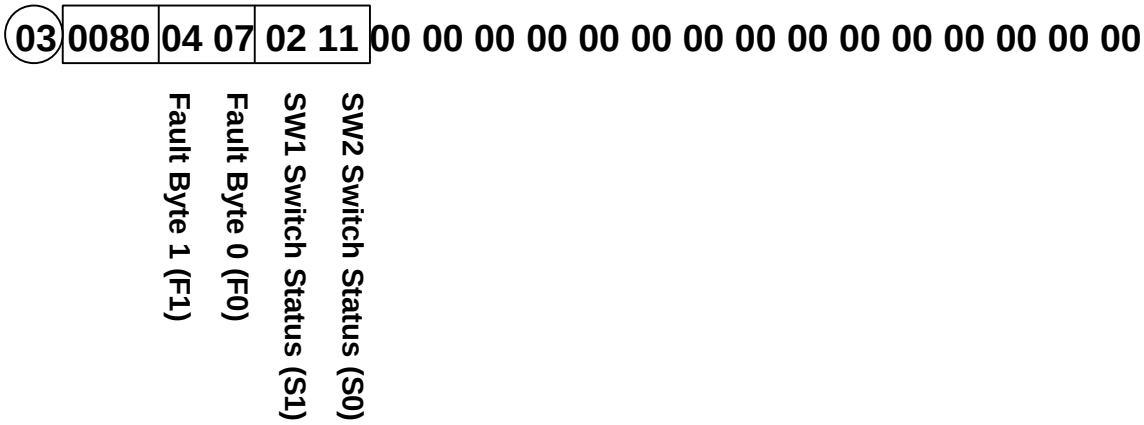
2.4.5 MACHINE REPORTS

The Fault Monitor CPU has another serial output mode called machine report mode. This mode is usually used with a computer program to interrogate the 56000 system status.
The machine report mode displays hexadecimal (HEX) characters like the verbose mode report.

The following is an example of a Fault Monitor CPU report in Machine Mode:

TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 00 80 04 07 0211 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)

Example from card slot 3 above:



Slot 3 shows that the Fault status is 0407 (F1, F0). The Status report read-out is 0201(S1,S0).

2.4.6 REPORT CONVERSIONS

This section deals with how to read and convert the Fault and Status read-outs using various tables and binary conversions. To decipher a Fault Status report, use Fig. A.
For Status reports (S1, S0) use Fig. B.

Fig. A

Spare	Spare	Spare	Spare	Primary Source	Sec. Input Fault****	Pri. Input Fault****	Power Cycled	Sec. Signal Loss****	Secondary BPV***	Secondary AIS**	Sec. E1/T1 Lockout**	Pri. Signal Loss****	Primary BPV***	Primary AIS**	Pri. E1/T1 Lockout*
8	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
0	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*1*	*1*
Upper Byte High Nibble				Upper Byte Low Nibble				Lower Byte High Nibble				Lower Byte Low Nibble			
0				**4**				**0**				**7**			

Fault Status F1 Report

Fault Status F0 Report

Key:

Above each 8,4,2,1 is the corresponding fault for that bit. For instance, above the 8 bit in the Upper byte/Low nibble reads Rub. Lockmon, which is the fault .

Shaded area
Informational only. The upper row: Bit value hex weights (8,4,2,1) The Lower row corresponds to the hex weight above. For instance, a readout of 7 equals 111 in binary and 4+2+1 hex weight. Each section of 8,4,2,1 is a nibble of either an Upper or Lower byte and separated for easy recognition. Each nibble = 4 bits and each byte = 8 bits. "04" is the F1 report, "07" the F0 report.

Non-shaded area
This area is used according with the report read-out after a report is converted to binary. The 0407 is an example from a report.

Always read the report from Upper (High) byte to Lower (Low) Byte.

* **Note 1** Refers to internal phase-locked-loop of the clock-extracting IC. (See theory of operation Section 3).

** **Note 2** Alarm Indication Signal: This is a standard data signature sent from upstream indicating an alarm.

***Note 3** Bipolar Violation: An indication that too many zeros are on the data stream. Please note that BPVs will only be detected if the 560-5208 is configured in T1 mode.

**** Latched Fault Bit -- Reset Via Fault Monitor CPU.

Always read the report from Upper (High) byte to Lower (Low) Byte.

Status (S1, S0) Conversion Table **FIG. B**

STATUS REG 0	Bit	Bit Value	Switch	
Low	0	1	SW 3-1 Enable	
Nibble	1	2	Secondary Disable SW 3-2	**1**
Low	2	4	SW3-3 (not used)	
Byte	3	8	SW 3-4 (not used)	
High	4	1	Ref Bus Select SQ SW 2-1	
Nibble	5	2	Ref Bus Select SQ SW 2-2	
Low	6	4	Ref Bus Select SQ SW 2-3	**1**
Byte	7	8	Output Inhibit SW 2-4	
STATUS REG 1				
Low	0	1	10 MHz Ref Freq SW 1-1	
Nibble	1	2	5 MHz Ref Freq SW 1-2	**2**
High	2	4	1 MHz Ref Freq SW 1-3	
Byte	3	8	E1/T1 Select SW 1-4	
High	4	1	Ref Bus Select Sine SW 4-6	
Nibble	5	2	Ref Bus Select Sine SW 4-7	
High	6	4	Ref Bus Select Sine SW 4-8	**0**
Byte	7	8	Not Defined	

Notes: The settings listed under the Switch column are HIGH or ON. For instance, frequency has SW 1-1 and SW 1-2. If SW 1-1 is ON, SW 1-2 is presumed to be OFF (although there is no specific mention of this). This is 10 Mhz. When SW1-2 is on, SW1-1 is off. This is 5 MHz. When both SW1-1 and SW1-2 are on, 1 MHz is active (on some boards). For switches, a 1 = ON, 0 = OFF.

Graphically, the switch settings look like this:

Switch/Position		10 MHz	5 MHz	1 MHz
1	1	1 (On)	0 (Off)	0
1	2	0 (Off)	1 (On)	0
1	3	(Off)	(Off)	1

Read from top to bottom for each MHz.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault
0 = No Fault

Use the Binary Conversion table to convert a read-out from the monitor to binary. For instance, if the report read-out was 3C15, this would be:

11\1100\1\101 in binary.

USING THE FAULT STATUS REPORT (F0,F1)

The hex weight has been assigned 8, 4, 2, 1. Beneath each number is the corresponding fault. Use Fig. A. The report example read 0407. The 0 is high byte/high nibble, the 4, high byte/low nibble, the 0, low byte/high nibble and 7, low byte/low nibble. Each nibble falls under a section on Fig. A, high to low or left to right.

Look at Fig. A. Below this is a sample read-out. This read-out would appear on the monitor when a Verbose report is requested. In the example, there are no faults in the upper byte/high nibble or in the lower byte/high nibble because both are zero (0). In the upper byte/low nibble, a 4 is reported. Looking directly above this, a 4 bit is easily spotted. The fault is Sec. Input Fault. However, In the lower byte/low nibble a 7 is reported. There is no 7 listed, only a 1, 2, 4, 8. Use the Binary Conversion table to determine the faults.

Seven (7) is converted to 111 in Binary. In Binary, a 1 = fault and 0 = no fault. Read 111 from bottom (low bit) to top (high bit) using the lower byte/low nibble group. The first three (from low bit to high bit) are 1's, indicating there is a fault with the Pri. BPV, Primary AIS, Pri. E1/T1 Lockout.

Note that the hex weight assigned totals to 7 (4+2+1). If the 7 had been a 6, in binary this is 110. Reading from low bit to high bit, the 1's (i.e., faults) fall under hex weight 4 and 2, which equals a hex weight of 6. Of

course, glancing at the lower byte/low nibble, you can quickly see (without converting to binary) that under 4 and 2 (i.e., 6) are the Pri. BPV and Primary AIS that are in fault.

Each of the four nibbles is grouped by category for easy visual identification of an offending fault. Each nibble has 15 possible fault combinations. All faults are asserted as a logic 1. The faults are latched on the Oscillator card and must be cleared by the 560-5179-1 Fault Monitor CPU "CL" command.

USING THE STATUS REPORT (S1, S0)

The method used for reading the Fault report is the same when reading the Status report. Refer to Fig. B.

Using the read-out, 0201, but because the table is different, the 0 is located at the bottom (high byte). The rest of the numbers follow upward towards the low byte (Status 0). In this case, the 2 falls in the low byte section of Status 1. The 1 falls in the low byte section of Status 0.

1 = Active, 0 = Not active.

Reading from high nibble to low nibble (in the Low Byte, Status 0) the current item is active:

SW 3-1 Enable	1
Sec. Disable SW 3-2	0
SW 3-3 (not used)	0

The 2 is converted to 10 in binary, indicating that SW1-2 (5 MHz) is active/on.

QUICK REFERENCE SHEET FOR READING FAULT AND STATUS REPORTS

1. Run a report. This is a portion of a sample Machine report.

TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 0080 04 07 0211 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)

0407 is the Fault Status read-out
0211 is the Status read-out report

04 = Fault Status 1 (F1) report
07 = Fault Status 0 (F0) report
02 = Status 1 (S1) report
11 = Status 0 (S0) report

03 0080 04 07 02 11 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Fault Byte 1 (F1)
Fault Byte 0 (F0)
SW1 Switch Status (S1)
SW2 Switch Status (S0)

What's in a number?

0 4 0 7

High Byte High Nibble — High Byte Low Nibble — Low Byte High Nibble — Low Byte Low Nibble

2. When required, convert Decimal to Binary using the Binary Conversion Table.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault/On/Active/YIN
0 = No Fault/Off/Not Active/YANG

SECTION THREE

3. THEORY OF OPERATION

3.1. GENERAL INFORMATION

This section contains a detailed description of the circuits used on the E1/T1 Reference Interface card.

3.2. HARDWARE DESCRIPTION

The E1/T1 Reference Interface incorporates two receive line interface chips, a DC-to-DC Converter and one phase-locked OCXO.

3.3. DETAILED DESCRIPTION

Reference drawing 560-5208.

3.3.1. DUAL RECEIVE LINE INTERFACES

Two receive line interface systems provide a means to interface bipolar E1 or T1 signals to a TTL digital system. Each of the two E1/T1 bipolar inputs are transformer coupled via 1:2 center-tapped transformers. The secondary sides of these transformers are provided jumper selectable resistors to properly terminate the lines with 100 ohms for T1 signals and 75 or 120 ohms for CEPT (E1) signals.

The secondary sides of the transformers are also connected to the RTIP and RRING (Receive Tip and Receive Ring) inputs of Receive Line Interface chips. From each of these signals, a Line Rate Clock is extracted by the receive line interface.

The Receive Line Interface provides signal status lines to detect frequency lock status, bipolar violations, alarm indication signals and receive carrier loss.

3.3.2. POWER SUPPLY

The DC-to-DC Converter, converts 48 VDC backplane power to local ±5 VDC power. A poly-fuse protects the backplane power bus from internal DC-to-DC shorts. A diode protects the card from a voltage polarity reversal in the event of an installation error while wiring the chassis to an external DC power source. During normal operation, an L-C filter minimizes switching noise coupled back into the backplane power bus. During live-extraction, a capacitor absorbs the inductive-kick of the opened circuit, minimizing contact-arcing. The -5 VDC output of the supply is loaded to provide a minimum load to improve output voltage regulation.

3.3.3. OVEN CONTROLLED OSCILLATOR

The card is equipped with one Voltage, operating at 10 MHz. The 10 MHz OCXO is phase locked to a 1.544 or 2.048 MHz reference frequency that is derived from E1/T1 inputs A and B. The FPGA provides the proper logic for the selected input signal and the 10 MHz on-board oscillator. The user selects the proper divide ratio to divide selected ET/T1 source by in order to provide the phase compare frequency via a dip switch. The phase comparison output from the loop filter integrator connects to the voltage control input on the 10 MHz OCXO closing the loop. Note that if all external frequency sources are lost, that this oscillator will continue to run and will serve as the on board reference.

3.3.4. OUTPUT BUFFERS AND FREQUENCY DIVIDERS

The FPGA contains a divide-by-two followed by a divide-by-five, which provides 5 MHz and 1 MHz, respectively. The resultant signal is distributed on FPGA outputs. These three identical signals are distributed collectively on tri-state buffers. One of these five signals will be switch selected. The signals are read by the FPGA and decoded to one static TTL high signal among five FPGA outputs. This signal enables one of the tri-state buffers which delivers the reference signal to the selected 56000 reference bus line.

For a 10 MHz output, all digital output buffers are tri-stated. The 10 MHz signal from the OCXO output is transformed into a sinewave and inserted onto the desired backplane buss line via a closed dip switch selection.

3.3.5. FPGA / CPU INTERFACE

The FPGA provides the timing and control signals for the E1/T1 Reference Interface. In a system that includes a Fault Monitor/CPU assembly, the FPGA is also the interface between the E1/T1 Reference Interface and the CPU. Certain features can only be utilized via the CPU.

SECTION FOUR

4. ADDITIONAL DOCUMENTS

4.1. 560-5208 ASSEMBLY DRAWING / BILL OF MATERIALS